REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

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Vendor item drawing

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PMIC N/A

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TITLE

MICROCIRCUIT, DUAL CHANNEL DIGITAL ISOLATOR, MONOLITHIC SILICON

SIZE	CODE IDENT. NO.	DWG NO.
A	16236	V62/12630

REV

PAGE 1 **OF** 13

AMSC N/A

5962-V005-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual channel digital isolator microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12630	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADuM1200-EP	Dual channel digital isolator

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	JEDEC MS-012-AA	Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage, (V_{DD1}, V_{DD2})	-0.5 V to +7.0 V	2/
Input voltage, (V_{IA}, V_{IB})	-0.5 V to V_{DDI} + 0.5 V	2/ 3/
Output voltage, (V_{OA}, V_{OB})	-0.5 V to V_{DDO} +0.5 V	2/ 3/
Average output current per pin (I_O)	-11 mA to +11 mA	4/
Common mode transients (CM_L, CM_H)	-100 kV/µs to +100 kV/µs	5/
Ambient operating temperature, (T_A)	-55°C to +125°C	
Storage temperature, (T_{ST})	-55°C to 150°C	

1.4 Recommended operating conditions.

Supply voltage, (V_{DD1}, V_{DD2})	2.7 V to 5.5 V	2/
Input signal rise and fall times	1.0 ms	
Operating temperature, (T_A)	-55°C to +105°C	

1.5 Package characteristics.

Resistance (Input to output), R_{I-O}	10^{12} Ω	6/
Capacitance (Input to output) C_{I-O}	1.0 pF	(at f = 1 MHz)
Input capacitance, C_I	4.0 pF	
Junction to case thermal resistance,(Side 1) θ_{JCI}	46 °C/W	7/
Junction to case thermal resistance,(Side 2) θ_{JCO}	41 °C/W	

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ All voltages are relative to their respective ground.
3/ V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
4/ See FIGURE 6 for maximum rated current values for various temperatures.
5/ Refers to common mode transients exceeding the absolute maximum ratings can cause latch up or permanent damage.
6/ The device is considered a 2-terminal device; Pin1, Pin2, Pin3, and Pin4 are shorted together, and Pin5, Pin6, Pin7, and Pin8 are shorted together.
7/ Thermocouple located at center of package underside.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Truth table. The truth table shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

3.5.6 Thermal derating curve. The thermal derating curve shall be as shown in figure 6.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions $4.5\ V \le V_{DD1} \le 5.5\ V$ $4.5\ V \le V_{DD2} \le 5.5\ V$ 2/	Limits			Unit
			Min	Typ	Max	
5 V OPERATIONS						
DC specifications						
Input supply current per channel, quiescent	$I_{DDI(Q)}$			0.50	0.60	mA
Output supply current per channel, quiescent	$I_{DDO(Q)}$			0.19	0.30	mA
Total supply current, two channels 3/						mA
DC to 2 Mbps						
V_{DD1} supply current	$I_{DD1(Q)}$	4/		1.1	1.4	
V_{DD2} supply current	$I_{DD2(Q)}$	4/		0.5	0.8	
10 Mbps						
V_{DD1} supply current	$I_{DD1(Q)}$	5/		4.3	5.5	
V_{DD2} supply current	$I_{DD2(Q)}$	5/		1.3	2.0	
25 Mbps						
V_{DD1} supply current	$I_{DD1(Q)}$	6/		10	13	
V_{DD2} supply current	$I_{DD2(Q)}$	6/		2.8	3.4	
Input currents	I_{IA}, I_{IB}		-10	+0.01	+10	µA
Logic high input threshold	V_{IH}		0.7 x 7/			V
Logic low input threshold	V_{IL}				0.3 x 7/	
Logic high output voltages	V_{OAH}, V_{OBH}	I_{OX} = -20 µA, $V_{IX} = V_{IXH}$	7/ - 0.1	5.0		
		I_{OX} = -20 µA, $V_{IX} = V_{IXH}$	7/ - 0.5	4.8		
Logic low output voltages	V_{OAL}, V_{OBL}	I_{OX} = 20 µA, $V_{IX} = V_{IXL}$		0.0	0.1	
		I_{OX} = 400 µA, $V_{IX} = V_{IXL}$		0.04	0.1	
		I_{OX} = 4 mA, $V_{IX} = V_{IXL}$		0.2	0.4	
Switching specifications						
Minimum pulse width 8/	PW			20	40	ns
Maximum data rate 9/			25	50		Mbps
Propagation delay 10/	t_{PHL}, t_{PLH}		20		45	ns
Pulse width distortion, $\lvert t_{PLH} - t_{PHL} \rvert$ 10/	PWD				3	
Propagation delay skew 11/	t_{PSK}				15	
Channel to channel matching 12/	t_{PSKCD}/t_{PSKOD}				3	
Output rise/fall time (10% to 90%)	t_R/t_F			2.5		
Common mode transient immunity						
Logic high output 13/	$\lvert CM_H \rvert$	$V_{IX} = V_{DD1}$, V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V	25	35		kV/µs
Logic low output 13/	$\lvert CM_L \rvert$	V_{IX} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V	25	35		
Refresh rate	f_r			1.2		Mbps
Dynamic supply current per channel 14/						
Input	$I_{DDI(D)}$			0.19		mA/Mbps
Output	$I_{DDO(D)}$			0.05		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2.7 V ≤ V_{DD1} ≤ 3.6 V 2.7 V ≤ V_{DD2} ≤ 3.6 V 15/	Limits			Unit
			Min	Typ	Max	
3 V OPERATION						
DC specifications						
Input supply current per channel, quiescent	$I_{DDI(Q)}$			0.26	0.35	mA
Output supply current per channel, quiescent	$I_{DDO(Q)}$			0.11	0.20	mA
Total supply current, two channels 3/						mA
DC to 2 Mbps						
V_{DD1} supply current	$I_{DD1(Q)}$	4/		0.6	1.0	
V_{DD2} supply current	$I_{DD2(Q)}$	4/		0.2	0.6	
10 Mbps						
V_{DD1} supply current	$I_{DD1(Q)}$	5/		2.2	3.4	
V_{DD2} supply current	$I_{DD2(Q)}$	5/		0.7	1.1	
25 Mbps						
V_{DD1} supply current	$I_{DD1(Q)}$	6/		5.2	7.7	
V_{DD2} supply current	$I_{DD2(Q)}$	6/		1.5	2.0	
Input currents	I_{IA}, I_{IB}		-10	+0.01	+10	µA
Logic high input threshold	V_{IH}		0.7 x 7/			V
Logic low input threshold	V_{IL}				0.3 x 7/	
Logic high output voltages	V_{OAH}, V_{OBH}	I_{OX} = -20 µA, V_{IX} = V_{IXH}	7/ - 0.1	3.0		
		I_{OX} = -20 µA, V_{IX} = V_{IXH}	7/ - 0.5	2.8		
Logic low output voltages	V_{OAL}, V_{OBL}	I_{OX} = 20 µA, V_{IX} = V_{IXL}		0.0	0.1	
		I_{OX} = 400 µA, V_{IX} = V_{IXL}		0.04	0.1	
		I_{OX} = 4 mA, V_{IX} = V_{IXL}		0.2	0.4	
Switching specifications						
Minimum pulse width 8/	PW			20	40	ns
Maximum data rate 9/			25	50		Mbps
Propagation delay 10/	t_{PHL}, t_{PLH}		20		55	ns
Pulse width distortion, $\|t_{PLH} - t_{PHL}\|$ 10/	PWD				3	
Propagation delay skew 11/	t_{PSK}				16	
Channel to channel matching 12/	t_{PSKCD}/t_{PSKOD}				3	
Output rise/fall time (10% to 90%)	t_R/t_F			2.5		
Common mode transient immunity						
Logic high output 13/	$\|CM_H\|$	V_{IX} = V_{DD1}, V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V	25	35		kV/µs
Logic low output 13/	$\|CM_L\|$	V_{IX} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V	25	35		
Refresh rate	f_r			1.1		Mbps
Dynamic supply current per channel 14/						
Input	$I_{DDI(D)}$			0.10		mA/Mbps
Output	$I_{DDO(D)}$			0.03		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 16/	Limits			Unit
			Min	Typ	Max	
MIXED 5V/3V or 3 V/5 V OPERATION						
DC specifications						
Input supply current per channel, quiescent	$I_{DDI(Q)}$					mA
5 V/3 V operation				0.50	0.6	
3 V/5 V operation				0.26	0.35	
Output supply current per channel, quiescent	$I_{DDO(Q)}$					mA
5 V/3 V operation				0.11	0.20	
3 V/5 V operation				0.19	0.25	
Total supply current, two channels 3/						mA
DC to 2 Mbps						
V_{DD1} supply current	$I_{DD1(Q)}$					
5 V/3 V operation		4/		1.1	1.4	
3 V/5 V operation		4/		0.6	1.0	
V_{DD2} supply current	$I_{DD2(Q)}$					
5 V/3 V operation		4/		0.2	0.6	
3 V/5 V operation		4/		0.5	0.8	
10 Mbps						
V_{DD1} supply current	$I_{DD1(Q)}$					
5 V/3 V operation		5/		4.3	5.5	
3 V/5 V operation		5/		2.2	3.4	
V_{DD2} supply current	$I_{DD2(Q)}$					
5 V/3 V operation		5/		0.7	1.1	
3 V/5 V operation		5/		1.3	2.0	
25 Mbps						
V_{DD1} supply current	$I_{DD1(Q)}$					
5 V/3 V operation		6/		10	13	
3 V/5 V operation		6/		5.2	7.7	
V_{DD2} supply current	$I_{DD2(Q)}$					
5 V/3 V operation		6/		1.5	2.0	
3 V/5 V operation		6/		2.8	3.4	
Input currents	I_{IA}, I_{IB}		-10	+0.01	+10	µA
Logic high input threshold	V_{IH}		0.7 x 7/			V
Logic low input threshold	V_{IL}				0.3 x 7/	
Logic high output voltages	V_{OAH}, V_{OBH}	I_{OX} = -20 µA, V_{IX} = V_{IXH}	7/ - 0.1	3.0		
		I_{OX} = -20 µA, V_{IX} = V_{IXH}	7/ - 0.5	2.8		
Logic low output voltages	V_{OAL}, V_{OBL}	I_{OX} = 20 µA, V_{IX} = V_{IXL}		0.0	0.1	
		I_{OX} = 400 µA, V_{IX} = V_{IXL}		0.04	0.1	
		I_{OX} = 4 mA, V_{IX} = V_{IXL}		0.2	0.4	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 16/	Limits			Unit
			Min	Typ	Max	
MIXED 5V/3V or 3 V/5 V OPERATION - Continued						
Switching specifications						
Minimum pulse width 8/	PW			20	40	ns
Maximum data rate 9/			25	50		Mbps
Propagation delay 10/	t_{PHL}, t_{PLH}		20		50	ns
Pulse width distortion, $\|t_{PLH} - t_{PHL}\|$ 10/	PWD				3	
Propagation delay skew 11/	t_{PSK}				15	
Channel to channel matching 12/	t_{PSKCD}/t_{PSKOD}				3	
Output rise/fall time (10% to 90%)	t_R/t_F					
5 V/3 V operation				3.0		
3 V/5 V operation				2.5		
Common mode transient immunity						
Logic high output 13/	$\|CM_H\|$	$V_{IX} = V_{DD1}$, V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V	25	35		kV/µs
Logic low output 13/	$\|CM_L\|$	V_{IX} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V	25	35		
Refresh rate	f_r					Mbps
5 V/3 V operation				1.2		
3 V/5 V operation				1.1		
Dynamic supply current per channel 14/						
Input	$I_{DDI(D)}$					mA/Mbps
5 V/3 V operation				0.19		
3 V/5 V operation				0.10		
Output	$I_{DDO(D)}$					
5 V/3 V operation				0.03		
3 V/5 V operation				0.05		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ All voltages are relative to their respective ground; all min/max specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V.

3/ The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present.

4/ DC to 1 MHz logic signal frequency.

5/ 5 MHz logic signal frequency.

6/ 12.5 MHz logic signal frequency.

7/ (V_{DD1} or V_{DD2}).

8/ The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

9/ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

10/ t_{PHL} propagation delay is measure from 50% level of the falling edge of the V_{IX} signal to the 50% level of the falling edge of the V_{OX} signal . t_{PLH} propagation delay is measure from 50% level of the rising edge of the V_{IX} signal to the 50% level of the rising edge of the V_{OX} signal.

11/ t_{PSK} is the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

12/ Codirectional channel to channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing directional channel to channel matching is the absolute value on the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

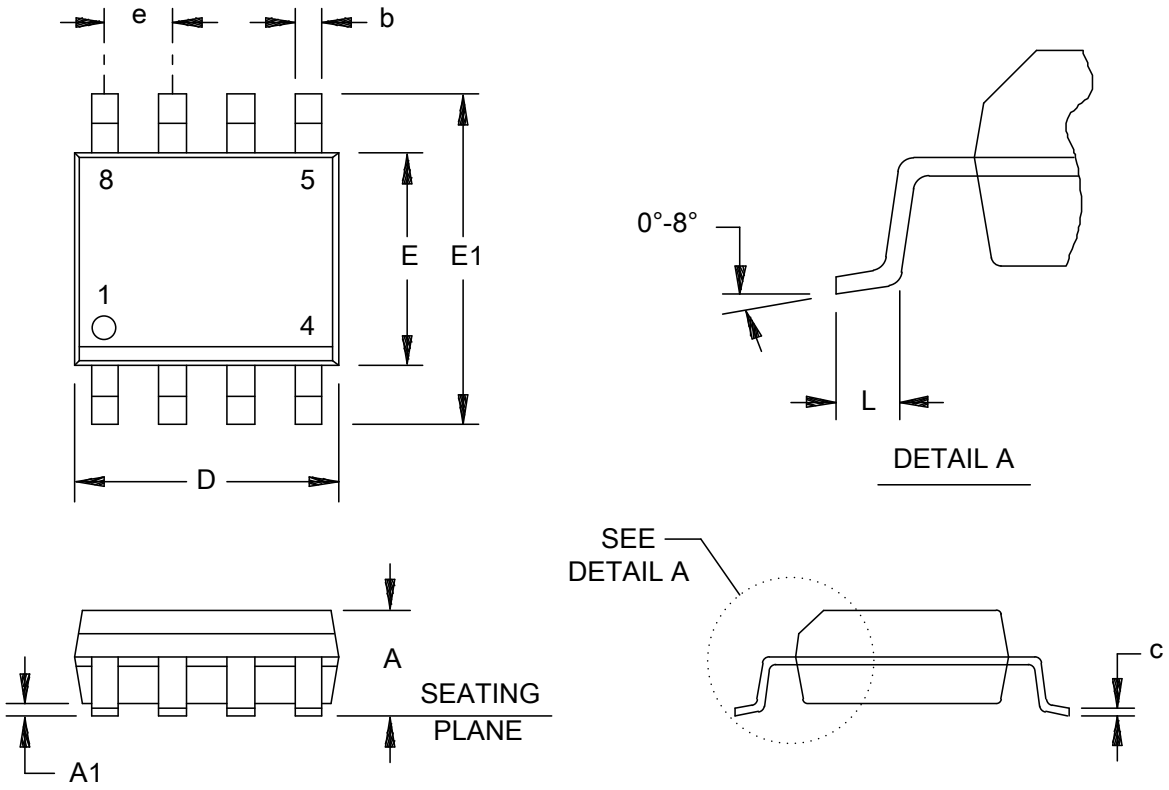
13/ CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining V_{OX} > 0.8 V_{DD2}. CM_L is the maximum common mode voltage slew rate that can be sustained while maintaining V_{OX} < 0.8 V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

14/ Dynamic supply current is the incremental amount of supply current required for a 1 MBps increase in the signal data rate.

15/ All voltages are relative to their respective ground; all min/max specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3 V.

16/ All voltages are relative to their respective ground; 5 V/3 V operation: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V. 3 V/5 V operation: 2.7 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all min/max specifications apply over the entire recommended operating range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = 3.0 V, V_{DD2} = 5.0 V; or V_{DD1} = 5.0 V, V_{DD2} = 3.0 V.

Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	1.35	1.75	.053	.068	E	3.80	4.00	.149	.157
A1	0.10	0.25	.004	.009	E1	5.80	6.20	.228	.244
b	0.31	0.51	.012	.020	e	1.27 BSC		.050 BSC	
c	0.17	0.25	.006	.009	L	0.40	1.27	.015	.050
D	4.80	5.00	.189	.196					

NOTES:
1. Controlling dimensions are in millimeters; inch dimensions (in parentheses) are rounded-off millimeter equivalents for reference only and are not appropriate for use in design.
2. Falls within JEDEC MS-012-AA.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{DD1}	5	GND_2
2	V_{IA}	6	V_{OB}
3	V_{IB}	7	V_{OA}
4	GND_1	8	VDD_2

FIGURE 2. Terminal connections.

Case outline X		
Terminal		Description
Number	Mnemonic	
1	V_{DD1}	Supply voltage for isolation side 1
2	V_{IA}	Logic input A.
3	V_{IB}	Logic input B.
4	GND_1	Ground 1. Ground reference for isolation side 1.
5	GND_2	Ground 2. Ground reference for isolation side 2.
6	V_{OB}	Logic output B.
7	V_{OA}	Logic output A.
8	VDD_2	Supply voltage for isolation side 2

FIGURE 3. Terminal function.

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} output	V_{OB} output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	H	H	1/
X	X	Powered	Unpowered	Indeterminate	Indeterminate	2/

1. Outputs return to the input state within 1 µs of V_{DDI} power restoration.
2. Outputs return to the input state within 1 µs of V_{DDO} power restoration.
3. H = High, L = Low, X = Undetermined/not relevant.

FIGURE 4. Truth table

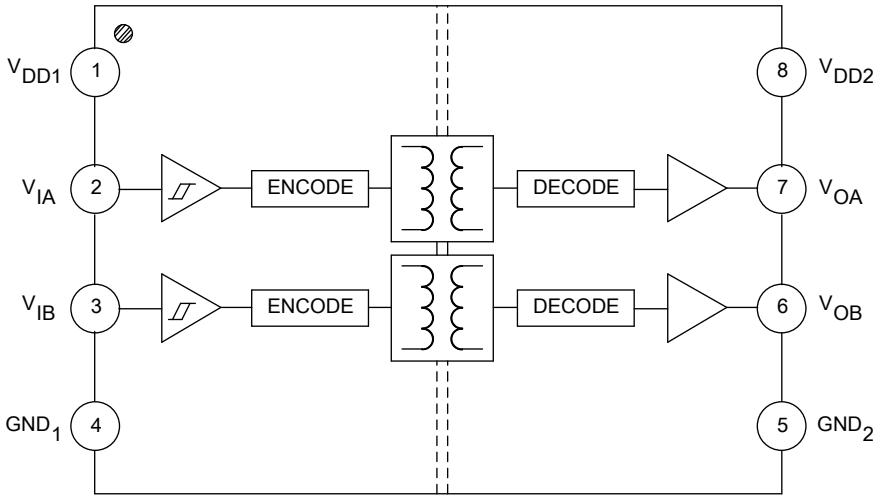


FIGURE 5. Functional block diagram.

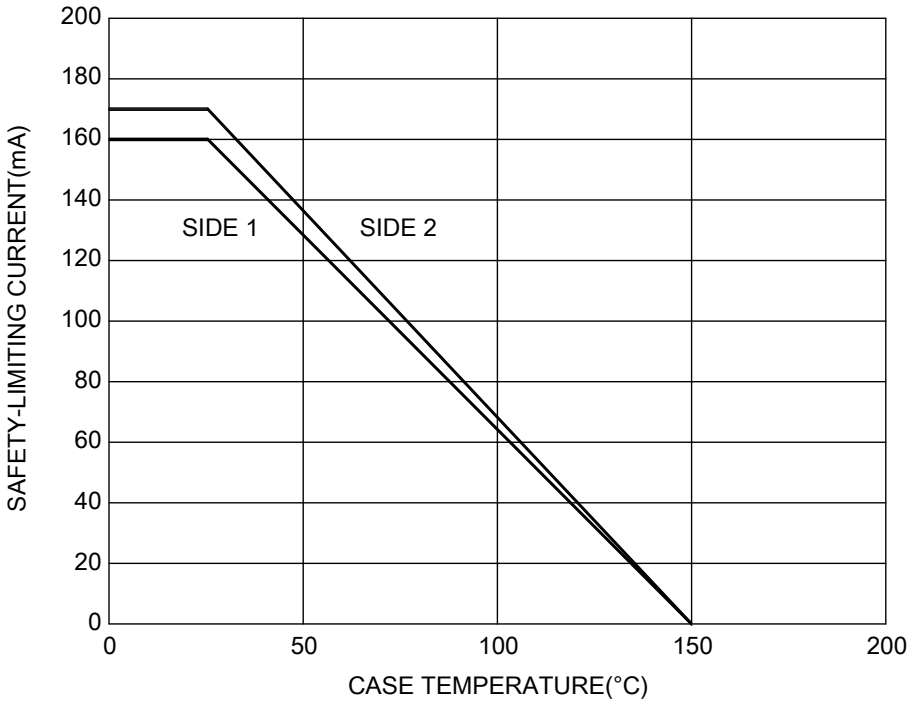


FIGURE 6. Thermal derating curve.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12630-01XB	24355	ADuM1200UR-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106